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IN THE CLAIMS

Claims 1-20 (Canceled).

21 (Previously Presented). A system comprising:

a controller to modify the address of a boot device;

a volatile memory coupled to said controller;

a bus coupled to said controller, said bus configured after the boot sequence; and

a programmable, non-volatile memory coupled to said bus, said memory storing system boot instructions.

22 (Previously Presented). The system of claim 21 wherein said system boot instructions include the basic input/output system.

23 (Previously Presented). The system of claim 22 wherein said non-volatile memory is a FLASH memory.

24 (Previously Presented). The system of claim 21 including a chipset coupled to said bus and having a general purpose output pin and an A20GATE pin, the general purpose output pin coupled to said A20GATE pin.

25 (Previously Presented). The system of claim 24 wherein said A20GATE pin is adapted to create a unique boot address for said non-volatile memory.